III. Amendments to the Claims

Claims 18-24 are pending in the present application. Claims 18-24 have been amended as set forth below. New Claims 47-70 have been added. This listing and version of the claims replaces all prior listing and versions of the claims.

1-17. (canceled)

18. (currently amended) An integrated vertical npn multiple transistor ESD protection structure on a semiconductor substrate, functionally connected to an integrated circuit input or output pin which will prevent electrostatic discharge damage to said integrated circuit comprising:[[;]]

a first semiconductor layer having a first conductivity dopant ~~dopent~~ type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopant ~~dopent~~ concentration;

a third semiconductor layer having a second conductivity dopant ~~dopent~~ type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopant ~~dopent~~ type laterally spaced from said first regions, being electrically connected to said third semiconductor layer

having a top element making electrical contact to said second regions and said second semiconductor layer; and

a plurality of third regions of said first semiconductor layer conductivity dopant ~~dopent~~ type laterally spaced and interposed between said second regions.[[;]]

19. (currently amended) The ESD protection structure of claim 18 whereby the plurality of first regions together with the associated connected first semiconductor layer are with n dopant ~~dopent~~ and form multiple collector elements of a bipolar transistor array in which ~~the~~ base elements of the bipolar transistor array ~~bases~~ are formed by said third conductivity layer and associated said plurality of second regions of p dopant ~~dopent~~, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions of n type dopant ~~dopent~~.

20. (currently amended) The ESD protection structure of claim 19 ~~18~~ whereby said ~~first~~ collector elements ~~regions~~ have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin and said base elements have horizontal conductor contact stripes.

21. (currently amended) The ESD protection structure of claim 19 ~~18~~ whereby said plurality of laterally spaced ~~pluralities of~~ third ~~emitter~~ regions by which said multiple emitter elements are formed are arranged in an alternating array within said third semiconductor ~~base~~ layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

22. (currently amended) The ESD protection structure of claim 20 ~~18~~ whereby one of said base horizontal conductor contact stripes ~~second semiconductor base horizontal contact region~~ lies between said top collector horizontal ~~collector~~ contact conductor stripe and said multiple emitter elements ~~contact regions~~, and a second of said base horizontal conductor contact stripes ~~semiconductor base horizontal contact region~~ lies between the bottom collector horizontal ~~collector~~ contact conductor stripe and said multiple emitter elements ~~contact regions~~ enabling surface connections to said base ~~regions~~ elements.

23. (currently amended) The ESD protection structure of claim 19 ~~18~~ whereby said ~~third semiconductor~~ multiple emitter elements ~~regions~~ are electrically connected by a contact conductor element with N horizontal stripe elements and connected in a contiguous serpentine manner by vertical contact conductor elements at alternate ends of respective ones of said N horizontal stripe elements ~~emitter conductor stripes~~.

24. (currently amended) The ESD protection structure of claim 22 ~~18~~ whereby said base horizontal conductor contact stripes ~~plurality of second semiconductor base region electrical contact conductor elements~~ and said multiple emitter elements ~~third semiconductor emitter region electrical contact conductors~~ are ultimately connected together and to a second voltage source~~, typically ground~~.

25-46. (canceled)

47. (new) The ESD protection structure of claim 24, wherein said second voltage is ground voltage.

48. (new) The ESD protection structure of claim 19, wherein said multiple emitter elements are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous box like manner by vertical contact conductor elements at both ends of respective ones of said N horizontal stripe conductor elements.

49. (new) The ESD protection structure of claim 19, wherein said multiple emitter elements are electrically connected by a conductor element with N horizontal stripe conductor elements

and connected in a contiguous comb like manner by a vertical contact conductor element at one end of respective ones of said N horizontal stripe conductor elements.

50. (new) The ESD protection structure of claim 23, wherein said and said base elements have horizontal conductor contact stripes, and said base horizontal conductor contact stripes are interdigitated between said N horizontal conductor stripe elements with the number of interdigitated based horizontal conductor stripes being equal to N+1.

51. (new) An integrated vertical npn multiple transistor ESD protection structure on a semiconductor substrate, functionally connected to an integrated circuit input or output pin which will prevent electrostatic discharge damage to said integrated circuit consisting essentially of:

a first semiconductor layer having a first conductivity dopant type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopant concentration;

a third semiconductor layer having a second conductivity dopant type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopant type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer; and

a plurality of third regions of said first semiconductor layer conductivity dopant type laterally spaced and interposed between said second regions,

wherein the plurality of first regions together with the associated connected first semiconductor layer form multiple collector elements of a bipolar transistor array in which base elements of the bipolar transistor array are formed by said third conductivity layer and associated said plurality of second regions, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions.

52. (new) The ESD protection structure of claim 51 whereby said collector elements have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin and said base elements have horizontal conductor contact stripes.

53. (new) The ESD protection structure of claim 52 whereby one of said base horizontal conductor contact stripes lies between said top collector horizontal contact conductor stripe and said multiple emitter elements, and a second of said base horizontal conductor contact stripes lies between the bottom collector horizontal contact conductor stripe and said multiple emitter elements enabling surface connections to said base elements.

54. (new) The ESD protection structure of claim 53 whereby said base horizontal conductor contact stripes and said multiple emitter elements are ultimately connected together and to a second voltage source.

55. (new) The ESD protection structure of claim 54, wherein said second voltage is ground voltage.

56. (new) The ESD protection structure of claim 51 whereby said plurality of laterally spaced third regions by which said multiple emitter elements are formed are arranged in an alternating array within said third semiconductor layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

57. (new) The ESD protection structure of claim 51 whereby said multiple emitter elements are electrically connected by a contact conductor element with N horizontal stripe elements and connected in a contiguous serpentine manner by vertical contact conductor elements at alternate ends of respective ones of said N horizontal stripe elements.

58. (new) The ESD protection structure of claim 57, wherein said and said base elements have horizontal conductor contact stripes, and said base horizontal conductor contact stripes are interdigitated between said N horizontal conductor stripe elements with the number of interdigitated based horizontal conductor stripes being equal to N+1.

59. (new) The ESD protection structure of claim 51, wherein said multiple emitter elements are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous box like manner by vertical contact conductor elements at both ends of respective ones of said N horizontal stripe conductor elements.

60. (new) The ESD protection structure of claim 51, wherein said multiple emitter elements are electrically connected by a conductor element with N horizontal stripe conductor elements

and connected in a contiguous comb like manner by a vertical contact conductor element at one end of respective ones of said N horizontal stripe conductor elements.

61. (new) An integrated vertical npn multiple transistor ESD protection structure on a semiconductor substrate, functionally connected to an integrated circuit input or output pin which will prevent electrostatic discharge damage to said integrated circuit comprising:

a first semiconductor layer having a first conductivity dopant type;

a second semiconductor layer overlying said first semiconductor layer, having a similar conductivity type as said first layer, but a different dopant concentration;

a third semiconductor layer having a second conductivity dopant type opposite that of said first semiconductor layer, disposed in overlying relation to said second semiconductor layer;

a plurality of first regions of said first conductivity type electrically connecting with said first semiconductor layer, having a top element making electrical contact to said first regions and said first semiconductor layer;

a plurality of second regions of said second conductivity dopant type laterally spaced from said first regions, being electrically connected to said third semiconductor layer having a top element making electrical contact to said second regions and said second semiconductor layer; and

a plurality of third regions of said first semiconductor layer conductivity dopant type laterally spaced and interposed between said second regions,

wherein the plurality of first regions together with the associated connected first semiconductor layer form multiple collector elements of a bipolar transistor array in which base elements of the bipolar transistor array are formed by said third conductivity layer and associated said plurality of second regions, and by which multiple emitter elements are formed by said plurality of laterally spaced third regions.

62. (new) The ESD protection structure of claim 61 whereby said collector elements have horizontal contact conductor stripes at the top and bottom of said transistor array which are ultimately connected together and to a first voltage source of said integrated circuit input/output pin and said base elements have horizontal conductor contact stripes.

63. (new) The ESD protection structure of claim 62 whereby one of said base horizontal conductor contact stripes lies between said top collector horizontal contact conductor stripe and said multiple emitter elements, and a second of said base horizontal conductor contact stripes lies between the bottom collector horizontal contact conductor stripe and said multiple emitter elements enabling surface connections to said base elements.

64. (new) The ESD protection structure of claim 63 whereby said base horizontal conductor contact stripes and said multiple emitter elements are ultimately connected together and to a second voltage source.

65. (new) The ESD protection structure of claim 64, wherein said second voltage is ground voltage.

66. (new) The ESD protection structure of claim 61 whereby said plurality of laterally spaced third regions by which said multiple emitter elements are formed are arranged in an alternating array within said third semiconductor layer, with "N" number of emitter regions whereby "N" corresponds to the number of multiple bipolar transistors in an electrically parallel transistor array that comprise said ESD protection structure.

67. (new) The ESD protection structure of claim 61 whereby said multiple emitter elements are electrically connected by a contact conductor element with N horizontal stripe elements and connected in a contiguous serpentine manner by vertical contact conductor elements at alternate ends of respective ones of said N horizontal stripe elements.

68. (new) The ESD protection structure of claim 67, wherein said and said base elements have horizontal conductor contact stripes, and said base horizontal conductor contact stripes are interdigitated between said N horizontal conductor stripe elements with the number of interdigitated based horizontal conductor stripes being equal to N+1.

69. (new) The ESD protection structure of claim 61, wherein said multiple emitter elements are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous box like manner by vertical contact conductor elements at both ends of respective ones of said N horizontal stripe conductor elements.

70. (new) The ESD protection structure of claim 61, wherein said multiple emitter elements are electrically connected by a conductor element with N horizontal stripe conductor elements and connected in a contiguous comb like manner by a vertical contact conductor element at one end of respective ones of said N horizontal stripe conductor elements.